AMENDMENTS IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE the paragraph beginning at page 14 line 17, with the following paragraph:

[0063] The offset region 730 has a zigzag shape and is a high resistance region, which may consist of low concentration impurity regions entirely or partially doped with impurities of the same conductivity types as the high concentration source/drain regions 721 and 725, or may consist of an intrinsic region undoped with impurities. The bottom left corner of the offset region 730 shown in Fig. 7A refers to a void area 731 relating to the zigzag shape of the offset region 730. As shown in the cross-sectional view of the thin film transistor of Fig. 7B, the offset region 730 has multiple void areas 731 related to the zigzag shape of the offset region 730.

Please REPLACE the paragraph beginning at page 12 line 13, with the following paragraph:

[0055] Referring to Fig. 6, the thin film transistor in the pixel portion includes a semiconductor layer 620 consisting of a polysilicon film, *etc.*, a gate electrode 640 and source/drain electrodes 651 and 655. The semiconductor layer 620 includes a channel region 624 corresponding to the gate electrode 640, and source/drain regions 621 and 625 formed at both sides of the channel regions 624. The source/drain electrodes 651 and 655 are electrically connected to the source/drain regions 621 and 625 through contacts 641 and 645.